WHAT IS CLAIMED IS:

1. A unified serial link system for transmitting digital data across wired media including a transmitter and a receiver,

the transmitter comprising a dual loop phase locked loop control circuit having a digital coarse loop for providing a PLL frequency control signal to an analog fine loop,

the receiver including a phase locked loop control circuit and an over sampled half-rate system comprising a signal edge comparator, an early/late signal generator based on the output of the comparator, and a multi-step phase rotator controlled by the generated signal.

2. The system according to claim 1 wherein the PLL in the transmitter is adapted to operate at full data rate and contains a four-stage voltage controlled oscillator adapted to run at full bit frequency.

3. The system according to claim 1 including a frequency reference clock that runs at one-fourth of the full data rate, and a comparator that compares the frequency of the PLL with the frequency of the reference clock.

4. The system according to claim 1 wherein the coarse loop includes a reference generator, a voltage comparator, a PLL control logic, a digital to analog counter and a low pass filter.

5. The system according to claim 1 wherein each of the transmitter PLL and the receiver PLL contains a pseudo random bit stream generator and checker for wrap mode self-testing.

6. The system according to claim 1 wherein the receiver includes a bit edge correlation table for generating early and late signals

7. The system according to claim 6 wherein a phase rotator control state machine is used to process the early and late signals from the correlation table to control the phase settings of the phase rotator.

8. The system according to claim 7 wherein the receiver phase rotator is independent of the receiver PLL, and is employed for the purpose of making phase adjustments and clock recovery.

9. The system according to claim 1 wherein the receiver PPL controls a voltage controlled oscillator, and the output phases of the oscillator are fed to the phase rotator.

10. The method of transmitting digital data across wired media between a transmitter and a receiver, comprising

providing a transmitter with a phase locked loop control circuit having a digital coarse loop and an analog fine loop,

providing a PLL frequency control signal from the coarse loop to an analog fine loop, and

providing a receiver including a phase locked loop control circuit and providing an over sampled half-rate system comprising a signal edge comparator, an early/late signal generator based on the output of the comparator, and a multi-step phase rotator controlled by the generated signal.

11. The method according to claim 10 wherein the PLL in the transmitter operates at full data rate and contains a four-stage voltage controlled oscillator running at full bit frequency.

12. The method according to claim 10 including a frequency reference clock that runs at one-fourth of the full data rate, and a comparator that compares the frequency of the PLL with the frequency of the reference clock.

13. The method according to claim 10 wherein the coarse loop further utilizes a reference generator, a voltage comparator, a PLL control logic, a digital to analog counter and a low pass filter.

14. The method according to claim 10 wherein each of the transmitter PLL and the receiver PLL uses a pseudo random bit stream generator and checker for wrap mode self-testing.

15. The method according to claim 10 wherein the receiver uses a bit edge correlation table for generating early and late signals.

16. Method according to claim 15 wherein a phase rotator control state machine process the early and late signals from the correlation table to control the phase settings of the phase rotator.

17. The method according to claim 16 wherein the receiver phase rotator is independent of the receiver PLL, and is employed for the purpose of making phase adjustments and clock recovery.

18. The method according to claim 10 wherein the receiver PPL controls a voltage controlled oscillator, and the output phases of the oscillator are fed to the phase rotator.

19. A unified system for transmitting and receiving data by a serial link across wired media, and comprising a transmitter and a receiver, the transmitter comprising:

a) phase locked loop control circuit having a digital coarse loop and an analog fine loop, the coarse loop including a reference generator, a voltage comparator, a PLL control logic, a digital To analog counter and a low pass filter;

b) a two-stage voltage regulated ring oscillator controlled by the phase locked loop,

and capable of running at full bit frequency;

c) a frequency reference operating at one-fourth of full data rate;

d) a reference clock and a phase locked loop clock;

the fine loop control formed by a 4x frequency divider, a phase-frequency detector, a charge pump and a loop file; and

the receiver comprising a phase locked loop including a voltage controlled oscillator, a phase rotator independent of the phase locked loop and adapted to receive the output phases of the oscillator, a phase rotator control state machine for controlling the phase setting of a phase rotator and employing an over sampled half-rate system using a digitized early-late control .

20. In the system according to claim 19, the transmitter and the receiver each includes a pseudo random bit stream generator and checker for self testing.

21. The system according to claim 20 wherein the transmitter architecture is supported by three analog blocks comprising the full data rate PLL, a phase buffer to

repower the PLL signal for the driver and an off chip driver with a pre-emphasis equalization.

22. A method of aligning the edges of a digitized baseband signal comprising:

a) sampling the signal;

b) generating an early or late signal when the signal is sampled early or late of the signal midpoint;

c) executing a command to change the sample timing in response to the generated signal, and

d) rotating the timing to adjust the sampling to the center of the signal.

23. The method according to claim 22 wherein the sample timing command is executed in response to a preponderance of early or late samplings.